

CLAIMS

What is claimed is:

1 1. A base station controller for a wireless network, comprising:

2 a plurality of processor boards, each processor board having a local timer; and

3 a plurality of timing units, each timing unit generating timing cells, each timing cell

4 containing time information, and each timing unit transmitting timing cells to each one of the
5 plurality of processor boards;

6 wherein a processor board realigns its local timer with time information contained in a
7 received timing cell whenever its local timer drifts from the time information contained in the
8 received timing cell by a predetermined time offset.

9 2. The base station controller of claim 1, wherein the predetermined time offset is
10 approximately 1 ms.

11 3. The base station controller of claim 1, wherein each processor board alternately
12 receives a timing cell from each one of the timing units.

1 4. The base station controller of claim 1, wherein the timing cells are transmitted to the
2 processor boards over an Asynchronous Transfer Mode (ATM) network.

1 5. The base station controller of claim 1, wherein the timing cells are transmitted to the
2 processor boards over an Ethernet network.

1 6. The base station controller of claim 1, wherein the timing cells are transmitted to the
2 processor boards over a universal serial bus.

1 7. The base station controller of claim 1, wherein a processor board does not realign its
2 local timer with time information contained in a received timing cell when a time difference between
3 its local timer and the time information contained in the received timing cell exceeds an error
4 threshold, the error threshold being greater than the time offset.

1 8. The base station controller of claim 7, wherein the error threshold is approximately 2
2 ms.

1 9. The base station controller of claim 3, wherein at least one of the processor boards
2 stores a fault status flag in a local memory, the fault status flag indicating a timing condition of the
3 respective processor board.

1 10. The base station controller of claim 9, wherein the fault status flag indicates an
2 inoperable timing condition of the respective processor board when time differences between the
3 respective local timer and time information contained in a received timing cell from each one of the
4 timing units exceed a predetermined error threshold.

1 11. The base station controller of claim 10, further comprising:

2 a main processor having a local database for periodically retrieving the fault status flag from
3 the processor boards and storing the retrieved fault status flag in the local database; and
4 a resource manager for assigning incoming calls to the processor boards based on the
5 retrieved fault status flag.

1 12. The base controller of claim 11, wherein the resource manager does not assign
2 incoming calls to a processor board when the retrieved fault status flag of the processor board
3 indicates an inoperable timing condition.

4 13. A method for distributing timing information to the processor boards in a base station
5 controller comprising a plurality of processor boards, each processor board having a local timer, and
6 a plurality of timing units, comprising the steps of:

7 generating timing cells from each one of the timing units, each timing cell containing time
8 information;

9 transmitting timing cells from each one of the timing units to each one of the processor the
10 processor boards; and

11 realigning the local timer of a processor board with time information contained in a received
12 timing cell when its local timer drifts from the time information contained in the received timing cell
13 by a predetermined time offset.

1 14. The method of claim 13, wherein the predetermined time offset is approximately 1
2 ms.

1 15. The method of claim 13 further comprising the step of alternately receiving a timing
2 cell at a processor board from each one of the timing units.

1 16. The method of claim 13, further comprising the step of transmitting the timing cells
2 to the processor boards over an Asynchronous Transfer Mode (ATM) network.

1 17. The method of claim 13, further comprising the step of transmitting the timing cells
2 to the processor boards over an Ethernet network.

1 18. The method of claim 13, further comprising the step of transmitting the timing cells
2 to the processor boards over a Universal Serial Bus.

1 19. The method of claim 13, further comprising the steps of not realigning the local timer
2 of a processor board with time information contained in a received timing cell when a time
3 difference between the local timer of the processor board and the received time information exceeds
4 a predetermined error threshold, the error threshold being greater than the time offset.

1 20. The method of claim 19, wherein the predetermined error threshold is approximately
2 2 ms.

1 21. A transceiver comprising:
2 a plurality of processor boards; and

3 a timing network containing a plurality of timing units, each timing unit continuously
4 providing a timing signal to each of the plurality of processor boards for setting a standard time.

1 22. The transceiver of claim 21, wherein each of the plurality of timing units provides its
2 respective timing signal at a different time so as to alternate the continuous timing signals from each
3 timing unit.

23. The transceiver of claim 22, wherein the timing signals are generated from a GPS
timing reference and are used to adjust a local timer in each one of the plurality of processor boards
to the standard time.

24. A wireless communication system, comprising:

a mobile station (MS); and

a base station (BS) in communication with the MS, the BS comprising:

a plurality of processor boards; and

a timing network containing a plurality of timing units, each timing unit continuously

providing a timing signal to each of the plurality of processor boards for setting a standard time.

1 25. The system of claim 24, wherein each of the plurality of timing units provides its
2 respective timing signal at a different time so as to alternate the continuous timing signals from each
3 timing unit.

1 26. The system of claim 25, wherein the timing signals are generated from GPS timing
2 reference and are used to adjust a local timer in each one of the plurality of processor boards to the
3 standard time.

09/24/2010 10:24:00 AM